UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,929	09/05/2003	Fadi Daou	3552.1001-001	8369

21005 7590 04/04/2007

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

EXAMINER	
PATHAK, SUDHANSHU C	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/656,929	DAOU, FADI	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Sept. 5th, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,11,21,22,26 and 27* is/are rejected.

7)☒ Claim(s) *4-10,12-20 and 23-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *Sept. 5th, 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-to-27 are pending in the application.

Specification

2. The disclosure is objected to because of the following:

The Abstract page recites the title of the invention; this should be removed.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 22 recites the limitation "the quantized amplitude value" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 21 (apparatus) & 26 (method), are rejected under 35 U.S.C. 103(a) as being unpatentable over Ward et al. (2003/0004664 A1) in view of Williams et al. (6,529,842).

In regards to Claims 1 & 26, Ward discloses an apparatus (method) for providing jitter measurement comprising: a sampling circuit for sampling an input signal to

obtain amplitude and phase information (Page 2, Paragraph 21, lines 1-4) {Interpretation: The reference discloses sampling the data waveform}; a computation circuit for computing Time Interval Error (TIE) information from the amplitude and phase information (Page 2, Paragraph(s) 21-22 & Fig. 1, element 110 & Fig.'s 2-3); and determining a jitter spectrum from the TIE information (Paragraph 18, lines 1-6 & Page 2, Paragraph 31, lines & Fig. 1, element 120 & Fig. 5, element 520). However, Ward does not explicitly disclose a signal processor for determining the signal spectrum.

Williams discloses a method and apparatus for measuring jitter (Column 2, lines 31-35). Williams further discloses a signal processor for determining the jitter spectrum (Column 3, lines 35-45 & Column 6, lines 24-57 & Fig. 2 & Fig. 15A). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Williams teaches a signal processor for determining the jitter spectrum and this is implemented in the apparatus as described in Ward so as to be able to store the incoming data and display the jitter spectrum.

In regards to Claims 2-3 & 27, Ward in view of Williams discloses an apparatus (method) for providing jitter measurement as described above. Ward further discloses a signal characteristics circuit for extracting characteristics of the input signal (Page 2, Paragraphs 23-25) {Interpretation: The reference discloses a circuit for extracting the signal characteristic includes a clock recovery circuit such as a PLL, as is also disclosed in the instant specification on Page 3, lines 1-6, which is used to compute the TIE}. Therefore, it would have been obvious to one of ordinary

skill in the art at the time of the invention that Ward in view of Williams satisfies the limitations of the claims.

In regards to Claims 21, Ward in view of Williams discloses an apparatus (method) for providing jitter measurement as described above. Ward further discloses the signal processor performs further analysis including determining peak-to-peak jitter or a ratio of random to deterministic jitter (Fig. 5, elements 560, 565 & Fig.'s 6 –7 & Fig. 8, elements 880-898 & Paragraph 44). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Ward in view of Williams satisfies the limitations of the claims.

7. Claim 11, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ward et al. (2003/0004664 A1) in view of Williams et al. (6,529,842) and further in view of Nayebi (5,291,074).

In regards to Claim 11, Ward in view of Williams discloses an apparatus (method) for providing jitter measurement as described above. However, Ward in view of Williams do not disclose the sampling circuit to include a Track and Hold (T/H) sampler that receives the input signal and the sample clock delayed by a fixed delay and provides amplitude samples to an A/D converter that generates quantized amplitude values corresponding to the amplitude samples.

Nayebi discloses a sampling circuit to include a Track and Hold (T/H) sampler that receives the input signal and the sample clock delayed by a fixed delay and provides amplitude samples to an A/D converter that generates quantized amplitude values corresponding to the amplitude samples (Column 1, lines 7-21). Therefore, it

would have been obvious to one of ordinary skill in the art at the time of the invention that Nayebi discloses a sampling circuit to include a Track and Hold (T/H) sampler that receives the input signal and the sample clock delayed by a fixed delay and provides amplitude samples to an A/D converter that generates quantized amplitude values corresponding to the amplitude samples and this is implemented in the apparatus as described in Ward in view of Williams so as to be able to digitize the incoming analog signal while reducing the aperture and sampling uncertainties thus increasing the speed and accuracy of the converter.

Allowable Subject Matter

8. Claims 4-10, 12-16, 17-20 & 23-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, it is recommended to the applicant to amend all the claims so as to be patentable over the cited prior art of record. A detailed list of pertinent references is included with this Office Action (See Attached "Notice of References Cited" (PTO-892)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (571)-272-3038. The examiner can normally be reached on M-F: 9am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571)-272-3042.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sudhanshu C. Pathak
Examiner
Art Unit 2611

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER